

FlexFPGA: A Case for Multi-Tenant Disaggregated **Cloud FPGA Architectures**

The Problem

- Traditional data centers restrict FPGA access to a single user, leading to resource underutilization and power wastage.
- FlexFPGA presents FPGAs as individual compute nodes integrated into data centers, enhancing efficiency, flexibility, and real-time resource allocation for diverse AI and cloud computing applications.





State of Research and Industry



Industry leaders like AWS, Alibaba, and Microsoft employ FPGA Co-Processor architectures, connecting FPGAs to hosts via PCIe, but still reserve them for single users, leading to potential resource and energy wastage.



ELECTRICAL & COMPUTER ENGINEERING

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FlexFPGA

- FlexFPGA is a research cloud FPGA architecture leveraging Zynq 7000 SoC and partial reconfiguration to treat FPGAs as stand-alone compute nodes, integrating them into data centers via network attachment.
- Multi-tenancy is enabled by allowing users to upload partial BIT streams and push them onto reconfigurable modules, presenting a unified FPGA space to users while utilizing multiple reconfigurable regions in the background.



Disaggregated Reconfigurable Hardware



Leveraging Zynq SoC and Dynamic Function Exchange

- Partial Reconfiguration preserves FPGA integrity while modifying specific areas with BIT files.
- FPGA shells can be created in Vivado and offer customizable infrastructure.
- Zynq 7000 devices integrate ARM Cortex-A9 processors with FPGAs, offering high performance and flexibility, suitable for seamless integration into data center and cloud environments with rich peripherals, facilitated by Xilinx's Vitis software platform.

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Multi-Tenancy



against traditional cloud computing architectures.





Future Work, References, and Acknowledgments

- Develop data center software architecture for multi-tenant su
- Gather additional power consu data for architecture analysis, comparing against traditional se
- Evaluate processing speed and scalability of the architecture a comparing with other alternativ

Methodology

• To evaluate the feasibility of our proposed architecture, we plan to measure processing speed and power consumption across disaggregated FPGAs and compare

Disaggregated Architecture Prototype

RM Shell 22:45 22:46 22:47 22:48 22:48 22:49 22:50 22:51 22:52 22:53 22:53 Power Consumption (W), FPGA with SoC Only

Power Consumption (W), FPGA with Prototype



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