ZeroScatterBLE: Zero-Added-Component Backscatter Communication using Existing FPGA Digital I/O Pins

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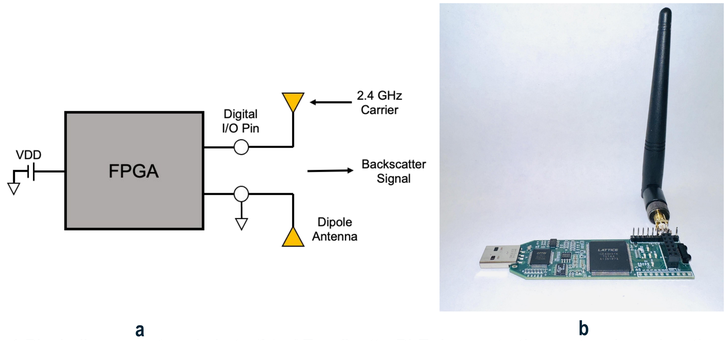
Overview

ZeroScatterBLE is an ultra-low-cost, zero-added-component approach that enables Bluetooth Low Energy (BLE) backscatter [1] wireless data uplink from billions of existing field-programmable gate arrays (FPGAs).

Current FPGA-based wireless sensors require either an external wireless communication chipset (e.g. BLE or WiFi), or additional external components for backscatter modulation (i.e RF FETS and PIN diodes). Previous work [2] demonstrated the use of existing digital I/O pins as backscatter modulators. This work shows that existing digital I/O pins on FPGA's can be used as FSK backscatter modulators capable of backscattering BLE-compatible data packets.



a b

Fig. 1 Block diagram **(a)** and photo **(b)** of ZeroScatterBLE demonstration system based on the Lattice iCE40HX1k FPGA demonstration board with 2.4GHz linearly polarized antenna

Digital I/O Pins as Backscatter Modulators

A typical on-chip digital I/O pin structure consists of a tri-state output driver combined with an input buffer. The key concept behind ZeroScatter is that digital pins with a selectable direction (input vs. output) present **two different RF impedances** with respect to ground, depending on the **pin direction**.

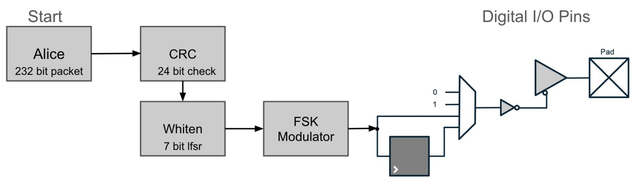


Fig. 2 Flow of "Alice" packet to FPGA I/O Pins

The block diagram above shows how the pre-coded "Alice" packet goes through a cyclic redundancy check, package contents are whitened, and finally put through an FSK modulator that outputs through the FPGA's digital I/O pins

	A	B	Pin State
Output mode	1	1	Output Low
	0	1	Invalid - Shorted VDD-GND
	0	0	Output High
Input mode	1	0	Tri-state Pin Floating

Fig. 3 Pinout chart

KEY CONCEPT Toggling a digital I/O pin between input and output modes presents **two distinct RF impedances**, enabling backscatter communication when the pin is directly connected to an antenna.

Experimental Setup

The setup includes a carrier source consisting of a signal generator operating at 2.4 GHz with a power level of +30 dBm connected to a 2.4GHz circularly polarized antenna. The backscatter tag is based on a Lattice Semiconductor ICE40HX1K FPGA connected to a 2.4GHz linearly polarized antenna. An unmodified iPad is used to receive the BLE backscatter signals.

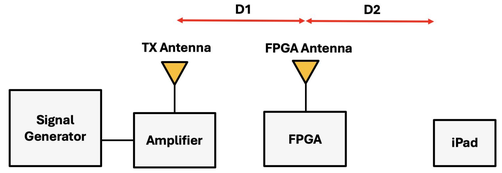


Fig. 4. Block Diagram of Experimental Setup

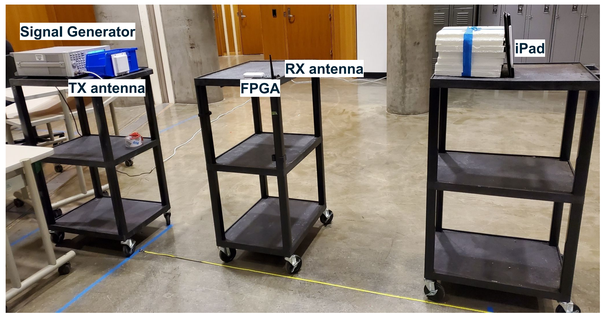


Fig. 5. Photo of Experimental Setup

Link Budget

The backscattered power available at the BLE tag is given by Eq. (1) where P_{out} is the power outputted by the signal generator. G_{TX} is the gain of the transmitting antenna on the FPGA. G_{D1} and G_{D2} is the free-space path gain between the signal generator and the FPGA and the FPGA and the receiver. G_{tag} is the gain of the tag, and G_{mod} is the internal modulation gain between the transmitting antenna and the FPGA.

$$iPad_{RSSI} = P_{out} + G_{TX} + G_{D1} + G_{tag} + G_{mod} + G_{tag} + G_{D2} \quad (1)$$

In this equation, all our variables are labeled as gains to not accidentally include a double negative in our calculations. Combining equations gives the backscattered power at the BLE receiver:

P_{out}	30.0 dBm	G_{tag}	2.14 dBi
G_{TX}	8 dBi	G_{mod}	-32.5 dBm
G_{D1}	-48 dBm	G_{D2}	-42 dBm

Table 1. Example set of parameters used for link budget calculation

Results

Fig. 6 presents the measured vs. expected backscatter power, calculated using the link budget of Eq. 1, with a CW source and iPad separated by 4 meters. The signal generator and the iPad are set at a fixed distance (4 m) while the FPGA with the RX antenna are moved by 0.1 m increments between them. The red plot is the measured results with the iPad scaling factor. The variation in measured received signal strength is due to multipath in the testing area.

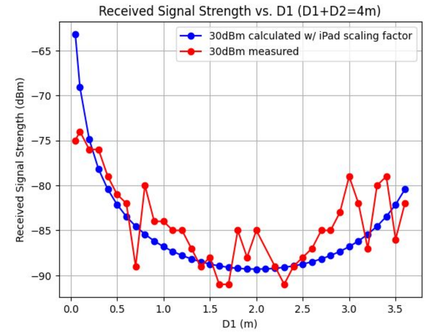


Fig. 6. Measured vs. Calculated received signal strength

The BLE packets sent from the FPGA to the iPad were generated using the method described in [1]. These packets were received by an Apple iPad running a commercial BLE Scanner app.

Fig. 7. BLE Packet received on iPad

BLE backscatter packets can be received by ***unmodified*** BLE devices

- Apple devices: iPad, iPhone, Mac
- Android devices
- PCs

Future Work

Future work will include increasing the capabilities of the design, including the creation of a general-purpose BLE telemetry block in Verilog that can be used to add BLE telemetry to other digital designs. This would allow a low cost and convenient wireless read-out of debugging and other data from existing FPGAs.

References

[1] J. Ensworth and M. Reynolds, "BLE-Backscatter: Ultra-low-power IoT nodes compatible with Bluetooth 4.0 Low Energy (BLE) smartphones and tablets", IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 9, pp. 3360-3368, 2017.

[2] A. Dadkhah, J. Rosenthal, M. Reynolds. "ZeroScatter: Zero-Added-Component Backscatter Communication using Existing Digital I/O Pins", IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNet), 2019.

[3] M. Woolley, et al. "Bluetooth® Core Specification Version 5.2 Feature Overview", 2020.